Amendments to the Claims:

Please replace paragraph [0006] with the following amended paragraph:

[0006] Figures 1 and 2 illustrate two different techniques for driving current into a low impedance write head. The write circuitry 110, 210 are used to drive current or a current step, ΔI_{OUT}, into write heads 116, 230, which are shown for simplicity as a short circuit. Each circuit 110, 210 includes a write driver 112, 212 for driving the head 116, 230 that is connected to the head 116, 230 through a transmission interconnect or electrical connection 114, 220 that is characterized by an odd characteristic impedance, Z_{ODD}, and a transmission delay, T_D, between the write driver 112, 212 and the head 116, 230. Figures 1 and 2 are drawn to show the write drive impedance conditions before the reflected signal that is generated on in the write head 116, 230 appears at the write driver 112, 212 side of the circuit 110, 210, which is typically twice the transmission delay or $2T_D$. The simplified circuits 110, 210 of Figures 1 and 2 allow the output current, ΔI_{OUT}, the write driver output voltage, ΔV_{IN}, and the power supplied by the write driver 112, 212 for the first $2T_D$ seconds after the transition to be calculated using well known equations governing the propagation of signals through a transmission line, e.g., ~~Equation 1~~ the power consumption equation provided ~~below~~ in the following paragraph. Also, the circuits 110, 210 include write driver generators that can be sized in order to have the same output current step, ΔI_{OUT}, to facilitate comparison of the circuits 110, 210.

Please replace paragraph [0007] with the following amended paragraph:

[0007] In circuit 110, the output impedance of the write driver 112 is much higher, e.g., considered to be infinite for simplicity, than the impedance, Z_{ODD}, of the interconnect 114 during the transition. The circuit 110 provides a technique for driving current with current source 113 through write head 116 that has the advantage of generating a current amplification effect on the load or head side

because the output current step, ΔI_{OUT}, is twice the source current step, $\Delta I_{IN}/2$. The amplification effect accounts for a gain in power of 2 or of 200 percent by the source for the first $2T_D$ seconds with respect to the circuit 210 of Figure 2, with power consumption determined by the following:

$$\text{Power Consumption} = DV_{IN} \cdot DI_{IN} = DI_{IN}^2 \cdot Z_{ODD} = (DI_{OUT} \cdot Z_{ODD})/4$$

Please replace paragraph [0009] with the following amended paragraph:

[0009] In circuit 210, the output impedance of the write driver 212 is set equal to the impedance of the transmission interconnect, Z_{ODD}, during the transition. The circuit 210 provides an advantage over the circuit 110 of Figure 1 in that write driver 212 [[an]] is impedance matched to the interconnect 220 via resistor 214. In this way, propagation of reflected waves is avoided when the current source 216 is used to drive the write head 230. The circuit 210 provides a clean output step, ΔI_{OUT}, in response to the input step, ΔI_{IN}, from current source 216. However, the circuit 210 does not provide any current amplification effect as is provided in the circuit 110 of Figure 1, as the output current step, ΔI_{OUT}, is equal to the source current step, ΔI_{IN}. As a result, during the period of twice the transmission delay, $2T_D$, after a transition, half of the current generated by the input source 216 flows away through the parallel path formed by the output impedance 214 of the write driver 212 and only half of the current is effectively launched into the line or interconnect 220, with power consumption determined by the following:

$$\text{Power Consumption} = DV_{IN} \cdot DI_{IN} = (DI_{IN}^2 \cdot Z_{ODD})/2 = (DI_{OUT}^2 \cdot Z_{ODD})/2$$

Please replace the paragraph [0031] with the following amended paragraph:

[0031] To control propagation of reflected waves from the head 328, the write driver [[334]] 330 also is shown to include an impedance matching circuit 334 to better illustrate the concept of matching impedance of the write driver 330 to the impedance of the interconnect 340. In practice, the circuit 334 may be included in

the voltage source circuit (or the power source may be considered part of the impedance matching circuit), with the important aspect being that the write driver 330 includes one or more components, such as resistors, that set the write driver 330 output impedance to the odd characteristic impedance of the interconnect 340 (where $Z_{ODD} = Z_O/2$). In other words, resistance of the driver 330 or R_{OUT} is selected to be equal to Z_{ODD} and power consumption for the write driver 330 can be determined with the equation of $(\Delta I_{OUT}^2 \cdot Z_{ODD})/4$ where ΔI_{OUT} is the current driven through the head 328.

Please replace the paragraph [0039] with the following amended paragraph:

[0039] As a result, the voltage step, ΔV_{IN}, is equal to the output voltage, HWX, of the driver [[410]] <u>510</u> to the interconnect 550 on node 522. Further, neglecting the bias of the buffer 530, the power consumption during the transition is given by the following formula:

$$POWER = (\Delta I_{OUT}^2 \cdot Z_{ODD})/2) \cdot (1/2 + 1/(2K))$$

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (original) A write driver for driving a write current through a write head, the write driver being connected to the write head by an interconnect having an odd characteristic impedance, the write driver comprising:

means for matching an output impedance of the write driver to the odd characteristic impedance of the interconnect; and

means for generating a source current output to the write head, wherein the write current is about twice the source current of the write driver, whereby power consumption of the write driver is one fourth of a product of the source current output and the odd characteristic impedance of the interconnect during a time period of twice a transmission delay of the interconnect.

2. (original) The write driver of claim 1, wherein the impedance matching means comprises an output resistor having a resistance substantially equal to the odd characteristic impedance of the interconnect.

3. (original) The write driver of claim 2, wherein the source current generating means comprises means for maintaining a voltage drop on the write driver output resistor at about zero for a period of twice a transmission delay of the interconnect.

4. (original) The write driver of claim 1, wherein the source current generating means comprises a transistor generating a pulsed current with an amplitude set by a current mirror connected to the transistor and by a reference current generator driving the current mirror.

5. (original) The write driver of claim 1, further comprising a voltage source comprising a buffer with unity gain connected to an input of the impedance matching means.

6. (original) The write driver of claim 5, wherein the voltage source further comprises a transistor and a resistor connected to an input of the buffer, the resistor having a resistance greater than the odd character impedance of the interconnect.

7. (original) A write assembly for a hard disk drive storing data on a disk, comprising:

a write head with a coil writing data to a surface of the disk in response to a write current passing through the coil;

an electrical interconnect connected to the write head coil, the interconnect comprising a transmission line having an odd characteristic impedance; and

a write driver connected to the interconnect generating an output current to drive the write current through the coil, wherein the write current is about twice the output current and wherein the write driver comprises an impedance matching circuit setting an output resistance of the write driver to about the odd characteristic impedance of the interconnect.

8. (original) The write assembly of claim 7, wherein the write driver comprises an output resistor with a resistance selected to define the output resistance of the write driver and wherein the write driver comprises a voltage source connected to the input of the output resistor.

9. (original) The write assembly of claim 8, wherein the voltage source comprises a buffer connected to an input of the output resistor and comprises a transistor and a resistor connected to an input of the buffer, the resistor having a resistance a scaling factor larger than the odd characteristic impedance of the interconnect.

10. (original) The write assembly of claim 9, wherein the write driver comprises a transistor generating the output current as a pulsed current, the output current transistor having a first area, and wherein the voltage source transistor has a second area defined by the first area divided by the scaling factor.

11. (currently amended) A write driver for selectively providing a write current through a write head in first and second opposite directions, the write driver being connected to the write head by an interconnect with an odd characteristic impedance, the write driver comprising:

a first current source connected to a first input of the interconnect providing a first source current step;

a second current source connected to a second input of the interconnect providing a second source current step, the first and second current steps each having a magnitude of about half the write current;

a first resistor connected to the first input of the interconnect having a resistance substantially equal to the odd characteristic impedance of the interconnect; [[and]]

a second resistor connected to the second input of the interconnect having a resistance substantially equal to the odd characteristic impedance of the interconnect[[.]] ; and

a differential voltage source comprising:

a first buffer connected to an input of the first current source and to an input of the first resistor;

a second buffer connected to an input of the second current source and to an input of the second resistor;

a first transistor connected to an input of the first buffer;

a second transistor connected to an input of the second buffer;

a third resistor connected to the input of the first buffer; and

a fourth resistor connected to the input of the second buffer.

Claim 12 (cancelled)

13. (currently amended) The write driver of claim [[12]] 11, wherein the third and fourth resistors have substantially equal resistances, and wherein each of the resistances of the third and fourth resistors is about equal to the odd characteristic impedance of the interconnect multiplied by a scaling factor that is greater than one.

14. (original) The write driver of claim 13, wherein each of the first and second current sources comprise a transistor and wherein the first and second transistors of the differential voltage source each have areas defined by dividing an area of one of the transistors of the current sources by the scaling factor.

15. (original) The write driver of claim 11, wherein the write driver is configured to have power consumption defined by the product of the square of the write current and odd characteristic impedance of the interconnect divided by four for a period of time equal to twice a transmission delay of the interconnect.

Claims 16-17 (cancelled)

18. (new) A write driver for selectively providing a write current through a write head in first and second opposite directions, the write driver being connected to the write head by an interconnect with an odd characteristic impedance, the write driver comprising:

a first current source connected to a first input of the interconnect providing a first source current step;

a second current source connected to a second input of the interconnect providing a second source current step, the first and second current steps each having a magnitude of about half the write current;

a first resistor connected to the first input of the interconnect having a resistance substantially equal to the odd characteristic impedance of the interconnect; and

a second resistor connected to the second input of the interconnect having a resistance substantially equal to the odd characteristic impedance of the interconnect,

wherein the write driver is configured to have power consumption defined by the product of the square of the write current and odd characteristic impedance of the interconnect divided by four for a period of time equal to twice a transmission delay of the interconnect.